

IST8101 ASIC for Residual current sensor Datasheet

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1. General Description

IST8101 is an ASIC chip to control and process the signal from magnetic current sensors. It enables the contact-free measurement of both the AC and DC current with high accuracy within the full operating temperature. With an intelligent switching design, IST8101 reduces the electrical offset and offset drift to an extremely low level.

IST8101 integrates multiple functions in one chip, which includes: multi-vibrator with duty cycle detection, digital-to-analog converter, fault detection, feedback and self-test circuits. It provides the analog output signal which is proportional to the primary current, the alarm flags and self-test functions compliance with both IEC 62752 and UL2231, overcurrent detection and reference output. IST8101 has embedded E-fuse memory to store the sensor parameters and chip configurations. IST8101 can also drive a feedback coil to achieve wide measurement range. I²C interface for digital output and communication is also available for various configurations' settings.

Features

- Drive and sensing the inductive magnetic sensor.
- Measure both the AC and DC current with high accuracy
- Intelligent switching design to utilize extremely low electrical offset.
- Analog and I²C digital output
- Alarm flags and self-test compliance with IEC 62752, IEC 62955 (hardware delay needed) and UL2231
- Single 5V supply
- Compact form factor, 4 x 4 x 0.9mm³, 32-pin QFN package

Applications

Residual current measurement in EV charge cable

Current sensing in green energy inverter systems

Leakage current measurement

System power consumption

Standard compliance

IEC 62752:2016

IEC62955:2018 –Hardware delay is needed

UL2231-2: 2nd Ed

AEC-Q100

2. Block Diagram, Package Dimensions and Application Circuits

2.1. Block Diagram

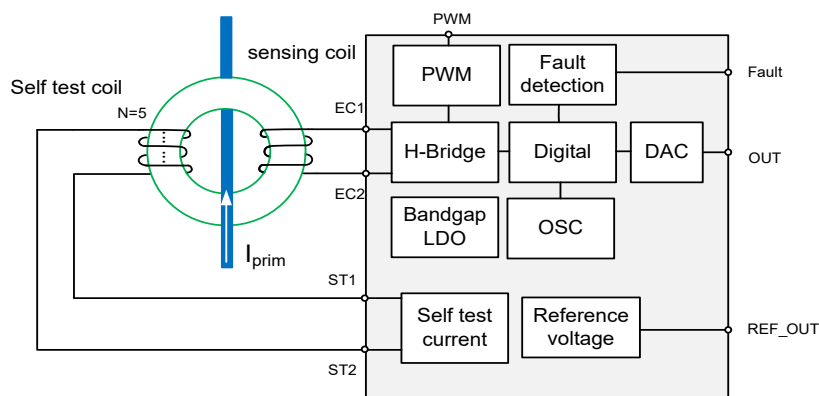
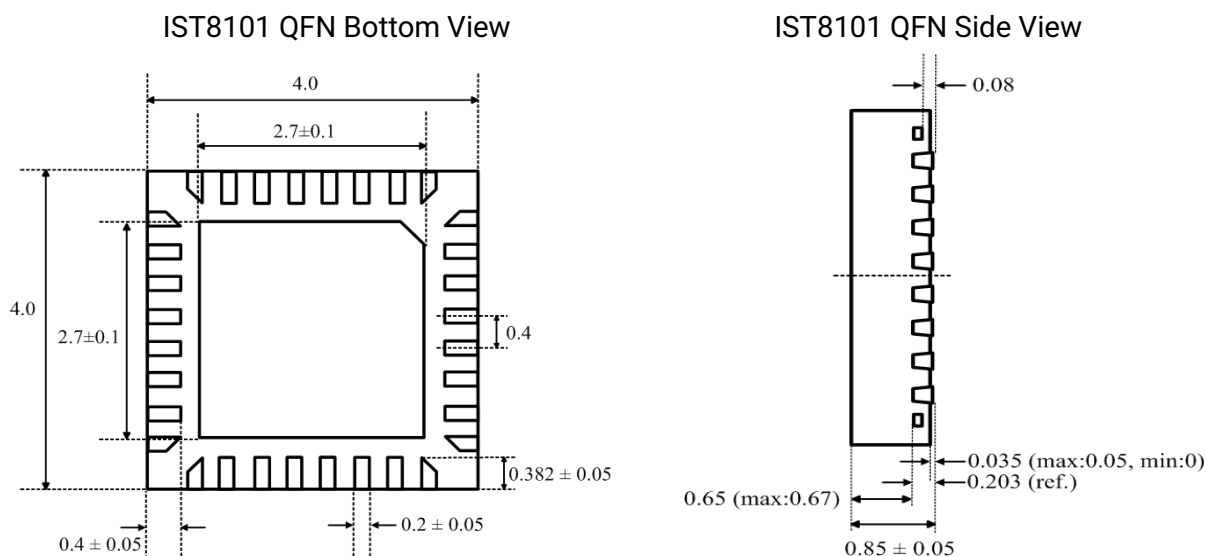


Figure 1. IST8101 Block diagram

2.2. Package and Pin Description

IST8101 utilizes a thermally enhanced QFN package with a built-in thermal pad, as depicted in Figure 2(a). The die is mounted on this thermal pad to enhance thermal conductivity, which is also connected to the GND pad. The exposed thermal pad on the bottom of package must be soldered onto the PCB and ground, as shown in Figure 2(b) layout recommendation. For optimal performance, place capacitor C1 as close as possible to pin 17 and pin 18, as they are regulator inputs. Similarly, position capacitor C7 nearest to pin 12 and pin 13, capacitor C8 closest to pin 14 and pin 15, and capacitor C6 closest to pin 16.



Unit: mm

Figure 2(a) IST8101 package

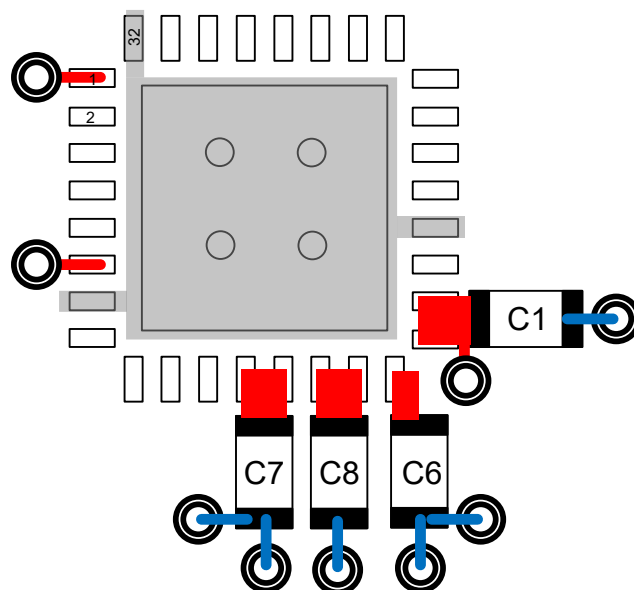


Figure 2(b). Layout recommendation

D=digital, A= analog, PWR= power, I= input, O=output, NC=no connection

Pin No.	Name	I/O Type	Description
1	VD5A	PWR	Input power
2	TC1	AI	Test coil connection
3	TC2	AI	Test coil connection
4	OUT	AO	DAC output
5	TESTA	DI	Enable selection of Test coil (internal pull down, 100KOhm)
6	VD5A	PWR	Input power
7	GNDA	PWR	VS_A, analog ground
8	REF_OUT	AO	2.25V output
9	REF_IN	AI	External reference voltage input
10	CLK_SEL	AI	Clock selection (internal pull down, 100KOhm) Low: internal clock High: external crystal (40MHz)
11	TST	AO	Analog test pin
12	VD_O	PWR	2.5V LDO input for OSC circuit
13	VD_D	PWR	2.5V LDO output for digital circuit
14	VIN	PWR	4.5V LDO input
15	VD_A	PWR	4.5V LDO output for analog circuit
16	VD_H	PWR	4.5V LDO output for H-Bridge

17	VD5A	PWR	Input power
18	VD5A	PWR	Input power
19	PWM	DO	Signal output
20	GNDA	PWR	VS_A, analog ground
21	EC2	AI	Sensor coil connection
22	EC1	AI	Sensor coil connection
23	XO	DO	Crystal OSC connection, NC
24	XI	DI	Crystal OSC connection, NC
25	NC		
26	HRESET	DI	Hardware reset; reserve for testing
27	OC	DO	Overcurrent alarm, active low
28	AC30mA	DO	AC 30mA alarm, active low (IEC62752) CCID20 alarm, active low (UL2231)
29	DC6mA	DO	DC 6mA alarm, active low (IEC62752) CCID5 alarm, active low (UL2231)
30	SDA	DIO	I ² C data, internal pull up resistor=74kOhm
31	SCL	DIO	I ² C clock, internal pull up resistor=74kOhm
32	GNDD	PWR	VS_D, digital ground

2.3. Application Circuit

IST8101 offers open-loop operation, which involves directly measuring the magnetic field generated by the primary current. The output signal is obtained from the OUT pin (Pin 4).

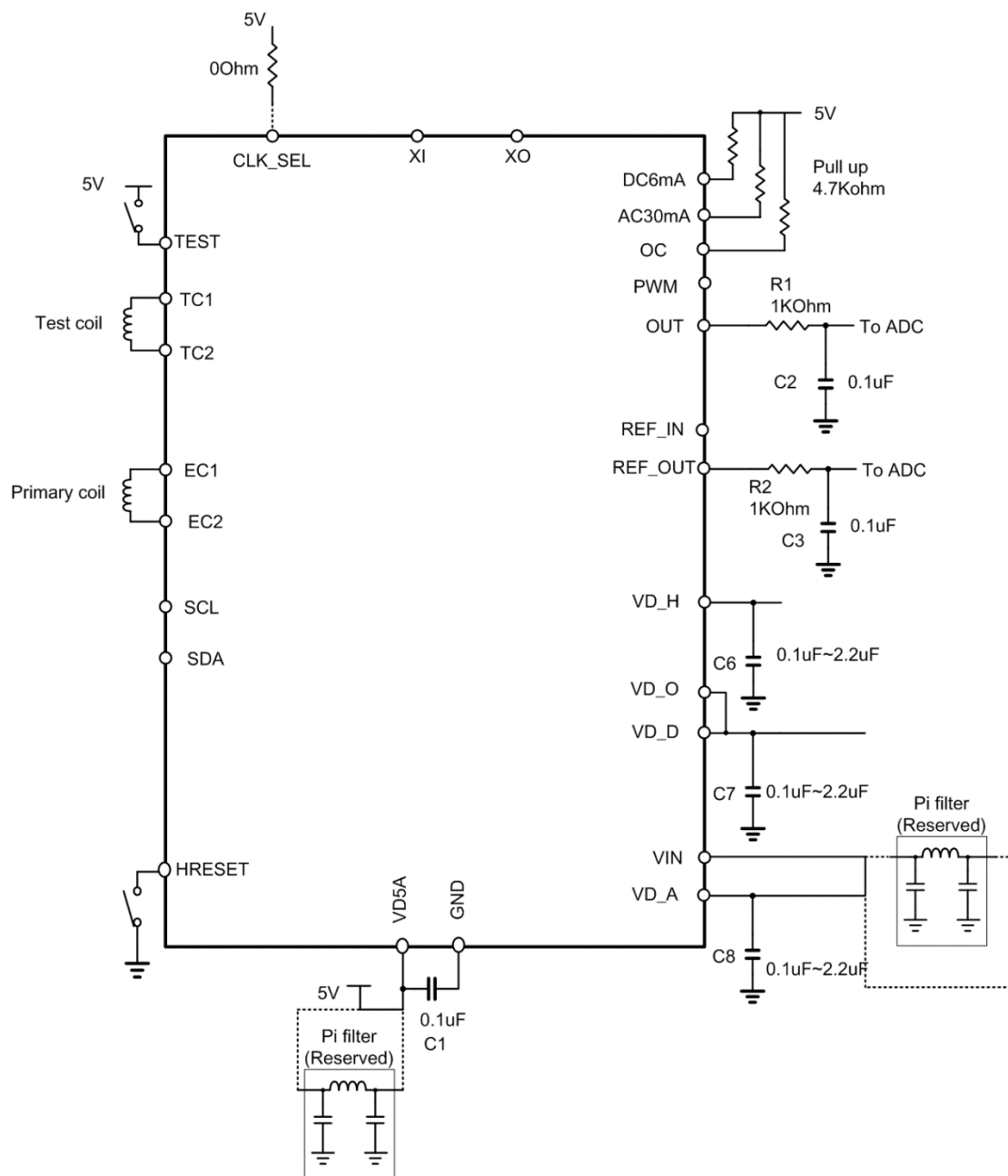


Figure 3. Application circuits for the open-loop operation.

C1, C6, C7 and C8 are decoupling capacitors that need to be closely connected to the chip pins.

3. Electrical Specifications

3.1. Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Supply Voltage	VDD	-0.3 to 6.0	V
Storage temperature	Ts	-40 to 150	°C
Electrostatic Discharge Voltage Human-body model (HBM)	VESD_HBM	±2000	V
Electrostatic Discharge Voltage Charged-device model (CDM)	VESD_CDM	-800 to 800	V

If the device is used in conditions exceeding these limits, it may cause permanent damage.

3.2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Temperature	TA	-40		125	°C
Power Supply Voltage	VDD	4.75	5	5.25	V

3.3. Electrical Specifications

Operating conditions: TA=+25°C; VDD=5V;

Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
Supply voltage	VD5A			5.0	6.0	V
Current consumption*1		ASIC+Coil, Rs=2050hm N=185		8.5	10	mA
Current consumption of ASIC		Not including coil		3.5	4	mA
Sensitivity*1		Rs=2050hm N=185	0.011	0.015	0.019	%/mA
Sensitivity drift $\Delta S/S$ over the temperature*2		No coil, No Temperature compensation, -40 ~ 125 °C		545	950	ppm/K

Fault detection of primary current (DC)	DC6mA	Alarm threshold of DC current, compliance with IEC62752:2016		3.5	4.75	6	mA
Fault detection of primary current (AC)	AC30mA	Alarm threshold of AC current (rms), compliance with IEC62752:2016		15	22.5	30	mA rms
DC Fault response time*1	DC6mA	6mA<DC<60mA			<1000		ms
		60mA<DC<300mA			<250		
		DC>300mA			<10		
AC Fault response time*1	AC30mA	30mA<AC<60mA(rms)			<250		ms
		60mA<AC<300mA(rms)			<100		
		AC>300mA			<10		
Fault detection of primary current	CCID5	Alarm threshold of CCID 5, compliance with UL2231	AC (60Hz)	4	5	6	mA rms
			DC Only		30		mA
Fault detection of primary current	CCID20	Alarm threshold of CCID 20, compliance with UL2231	AC (60 Hz)	15	17.5	20	mA rms
			DC Only		40×1.414		mA
Duty cycle noise*1	DCN	Rs=1040hm, No average Sen=5.5count/mA Sen= 0.18mA/count			0.36	0.72	mA(rms)
		Rs=2050hm, No average Sen=9.5count/mA Sen= 0.105mA/count			0.2	0.4	mA(rms)
Measurement range*1	mA	Rs=2050hm N=185		1		300	mA

Note.

*1: The parameters are dependent on the magnetic core.

*2: The sensitivity drift includes the resistor (R_s), the chopper switches and the H-bridge switches.

4. Functional Description

With a single 5V power supply and connecting to the magnetic sensor via EC1 and EC2 pins, IST8101 drives the magnetic sensor with a multi-vibrator circuit and generates the output signal proportional to the primary current. IST8101 provides the fault alarms when the primary current is over the thresholds defined by IEC 62752:2016, UL2231-2: 2nd Ed, or IEC 62955: 2018 (with properly designed hardware delay and register setting).

4.1. Fault Detection

The fault detection circuit processes the count signal to the AC and DC signal separately and compares with the thresholds. The alarm flags (DC6mA, AC30mA, OC) are pulled low when these signals become larger than the threshold settings, respectively. The alarm pins of DC6mA and AC30mA are configured by the option of IEC62752, UL2231 and hybrid mode as table below.

Alarm options for IEC62752, UL2231 and Hybrid mode

Pin Name	IEC62752	UL2231	Hybrid
DC6mA	DC6mA	CCID5	DC6mA
AC30mA	AC30mA	CCID20	CCID20

4.1.1. DC and AC Current Alarms for IEC62752

When the DC current value is over 6mA, the alarm flag of DC6mA turns to the low level (active low) with the response time respectively, as table below and Figure 4. During the range of $3\text{mA} < \text{DC} < 6\text{mA}$, the alarm status of DC6mA is uncertain (low or high) due to the measurement tolerance within the full operation range.

Input signal	Output Pin	Output Status	Response time	Description
$\text{DC} < 3\text{mA}$	DC6mA	High		Not Fault alarm
$6\text{mA} < \text{DC} < 60\text{mA}$	DC6mA	Low	$< 1000\text{ms}$	Fault alarm
$60\text{mA} < \text{DC} < 300\text{mA}$	DC6mA	Low	$< 250\text{ms}$	Fault alarm
$\text{DC} > 300\text{mA}$	DC6mA	Low	$< 10\text{ms}$	Fault alarm

Note: The alarm setting and response time are compliance with IEC 62752:2016.

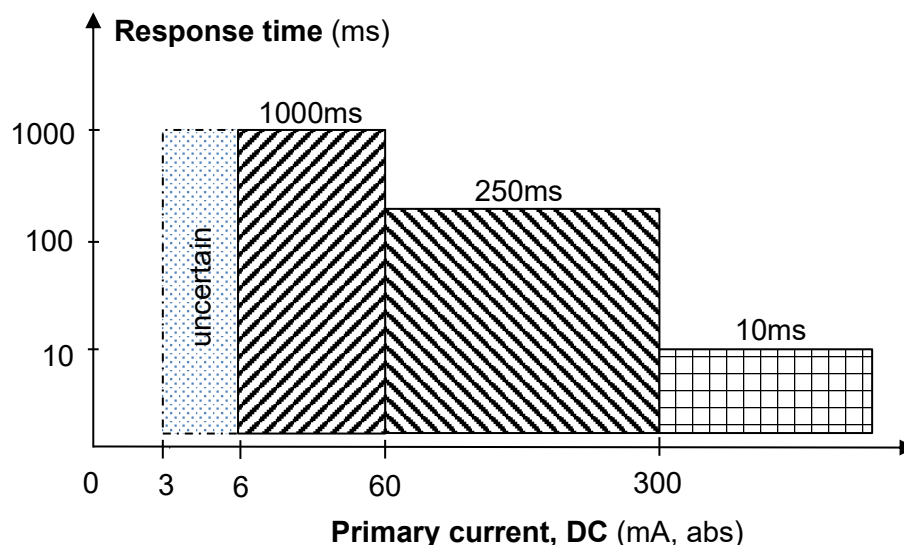


Figure 4. The alarm status of DC6mA and response time.

When the AC current becomes larger than 30mA, the alarm flag of AC30mA turns to low level (active low). The response time for different range of AC current is described as the table below and Figure 5. The uncertain status of AC30mA flag is $15\text{mA} < \text{AC} < 30\text{mA}$.

Input signal	Output Pin	Output Status	Response time	Description
$\text{AC} < 15\text{mA (rms)}$	AC30mA	High		Not Fault alarm
$30\text{mA} < \text{AC} < 60\text{mA (rms)}$	AC30mA	Low	$< 250\text{ms}$	Fault alarm
$60\text{mA} < \text{AC} < 300\text{mA (rms)}$	AC30mA	Low	$< 100\text{ms}$	Fault alarm
$\text{AC} > 300\text{mA (rms)}$	AC30mA	Low	$< 10\text{ms}$	Fault alarm

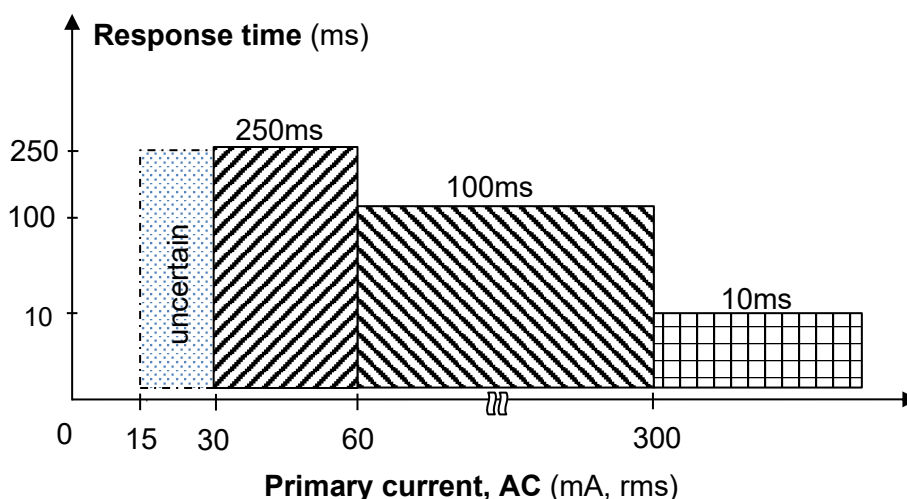


Figure 5. The alarm status of AC30mA current and response time.

4.1.2. Alarms for UL2231

According to UL2231, when the primary current reaches or exceeds the threshold as

described in Figure 6, IST8101 informs the charging circuit interrupting device (CCID) within the defined time. 2 alarms are designated as Type CCID5 and CCID20, where CCID is the composite AC & DC current in mA peak.

Alarm thresholds of CCID for AC or DC only

Type of Primary current	CCID5	CCID20
AC (60Hz) only	5±1mA (rms)	15 to 20mA (rms)
DC only	30mA	40 × 1.414 mA

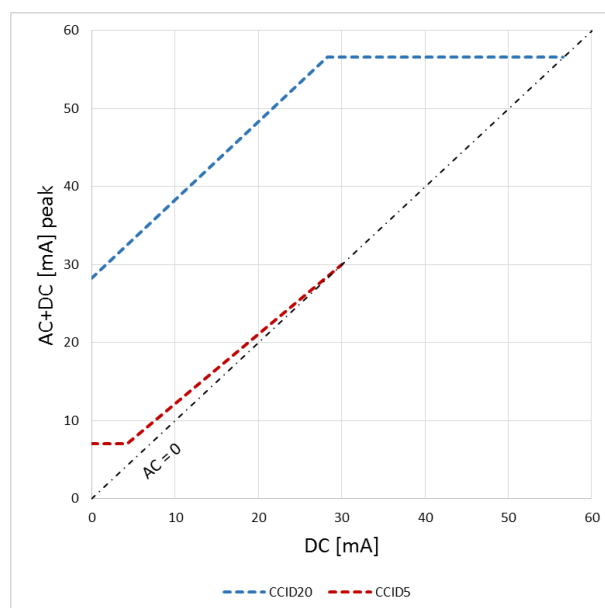


Figure 6. Alarm threshold for Type CCID5 and CCID20 (UL2231).

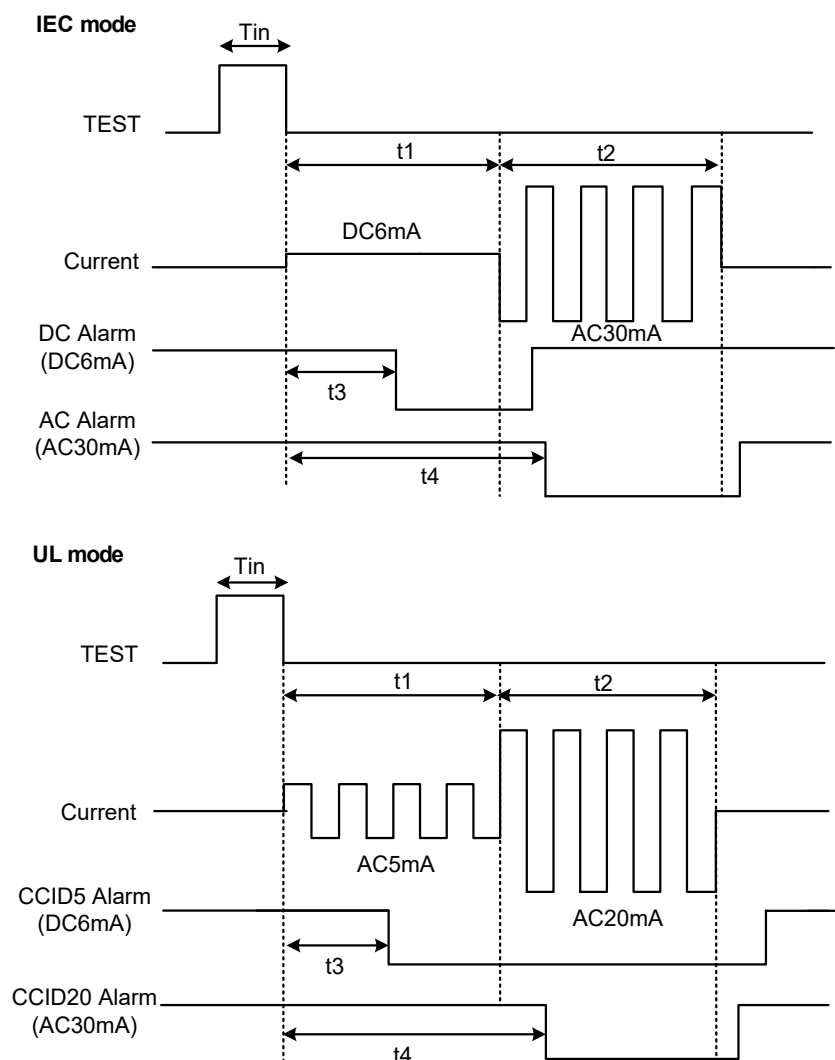
4.1.3. Over-current Detection of the Magnetic Sensor

When the primary current is larger than 200mA (DC) or 300mA (AC, rms), it is overloading and the OC pin (pin27) is pulled to low level (active low) as an alarm flag. The overloading is also active when the oscillation frequency of the H-bridge is larger than a certain threshold or lower than 200Hz.

Input signal	Output Pin	Output Status	Description
DC > 200mA or AC > 300mA (rms)	OC	Low	Fault alarm
Oscillation frequency > threshold	OC	Low	Fault alarm
Oscillation frequency < 200Hz	OC	Low	Fault alarm

4.2. Self-test Function

A self-test function is designed in IST8101 to detect whether the sensor operates as the requirements or fails. When the self-test function is enabled by the Test pin and connects the TC1 and TC2 pin with a test coil, IST8101 generates a driving current to the test coil which produces a magnetic field. This magnetic field emulates the existence of a primary current. There are 3 modes for the self-test as IEC, UL and Hybrid mode. Figure 7 shows the 3 modes when the 0x37[6] is 0 (alarm active low). The self-test is triggered at the falling edge of an external pulse signal with a duration $T_{in} > 120\mu s$. The testing time of t_1 and t_2 are both 0.8s, and the AC frequency is 60Hz. If the sensing output is within the expected range, it indicates that the sensor operates properly and the self-test is passed.



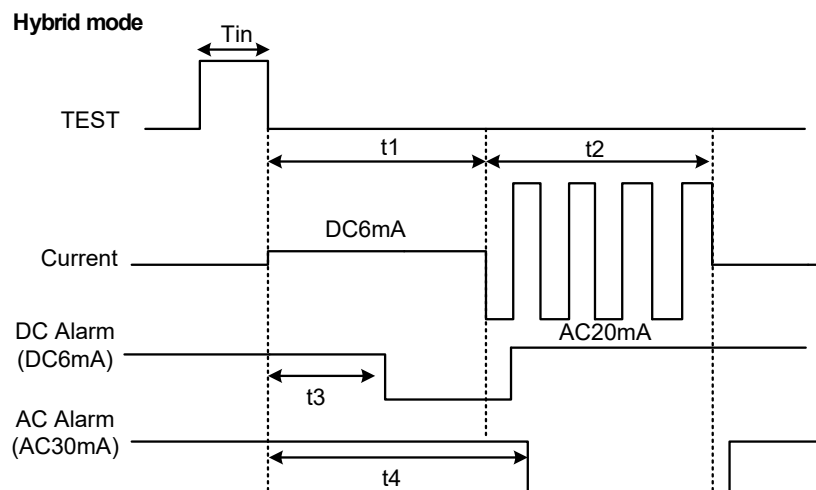


Figure 7. Self-test function, when 0x37[6] is 0

Variation range of t1, t2, t3, t4 and T_{in}

Parameter	Min	Typ	Max
t1	0.696s	0.80s	0.904s
t2	0.696s	0.80s	0.904s
t3 ^{*1}	0.22s	0.26s	0.3s
t4 ^{*1}	0.84s	1s	1.16s
T_{in}	120us		-

The t1 and t2 have a 13% variation, which includes the clock drift at temperature (8%) and the clock tuning variation (5%).

^{*1} t3 and t4 are magnetic core dependent.

4.3. Power-Up Rise Time

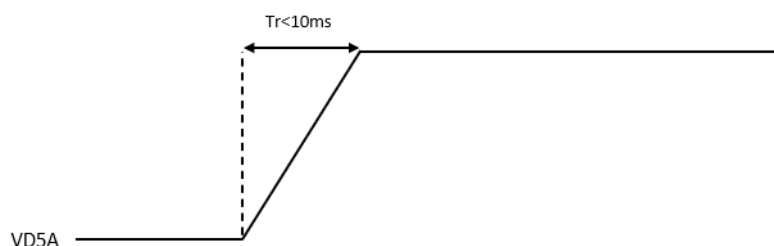


Figure 8. Power-Up Rise Time

5. Digital Interface

5.1. I²C Interface

The interface of IST8101 follows the standard I²C definition guidelines with some additional protocol definitions. IST8101 supports standard speed (100kHz) and fast speed (400kHz). The pull-up resistors of 4.7kohm for both SDA and SCL lines should be used.

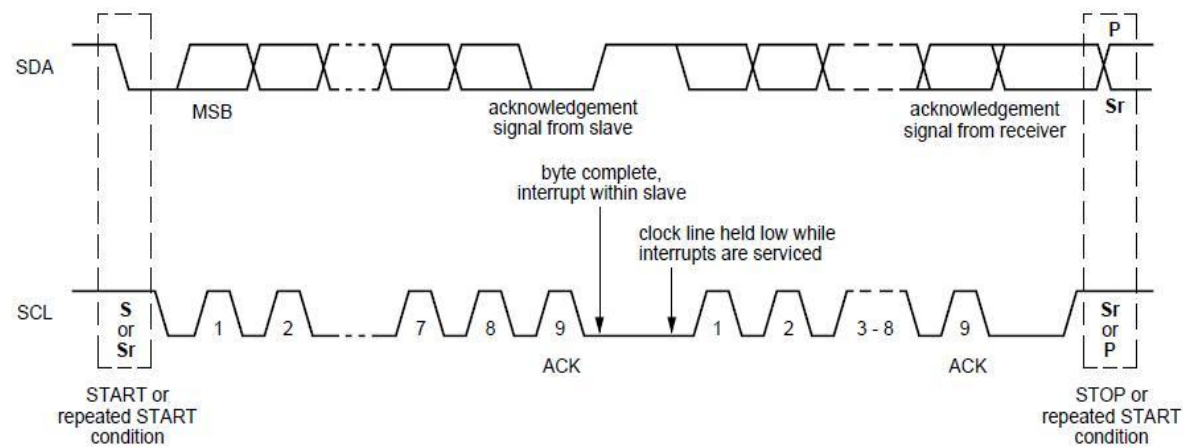


Figure 9. I²C Operation

5.1.1. Slave Address

MSB				LSB			
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	1	0	0	R/W

IST8101 uses 7-bit slave address as 0CH. If user uses 8-bit address; the slave address is 18H.

5.1.2. I²C Read Operation

Single-Byte Read:

SA	Slave Address+W	ACK	Reg Address	ACK	SP	Slave Address+R	ACK	DATA	NA	ST
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I²C Single-Byte Read Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master □: Master to Slave

Multiple Byte Read:

SA	Slave Address+W	ACK	Reg Address	ACK	SP	Slave Address+R	ACK	DATA	ACK	DATA	NA	ST
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I²C Multiple Byte Read Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master : Master to Slave

5.1.3. I²C Write Operation

Single-Byte Write:

SA	Slave Address+W	ACK	Reg Address	ACK	DATA	ACK	ST
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I²C Single-Byte Write Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master : Master to Slave

Multiple Byte Write:


SA	Slave Address+W	ACK	Reg Address	ACK	DATA	ACK	DATA	ACK	ST
----	-----------------	-----	-------------	-----	------	-----	------	-----	----

I²C Multiple Byte Write Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master : Master to Slave

6. Ordering Information

Order Number	Package Type	Packaging	
IST8101	QFN-32 pin	Tape and Reel: 3k pieces per reel	 <p>8101: Product Code Y: Last number of the year WW: week number (Week of January 1 is week "01")</p>

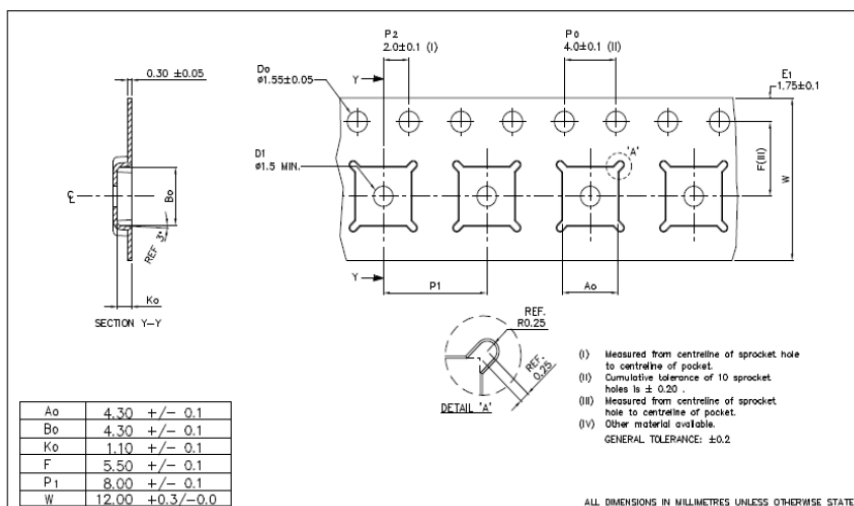
6.1. Package Information

Using 13" 4Hub Reel- [No 7" reel for such carrier width]

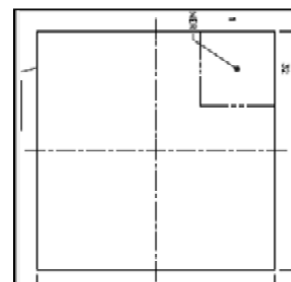
Max MPQ: 3K/per reel under leader-400mm/trailer-160mm Pin1

Orientation: Based on EIA-481 will follow as upper-right

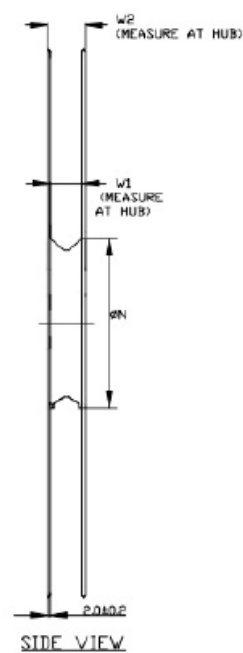
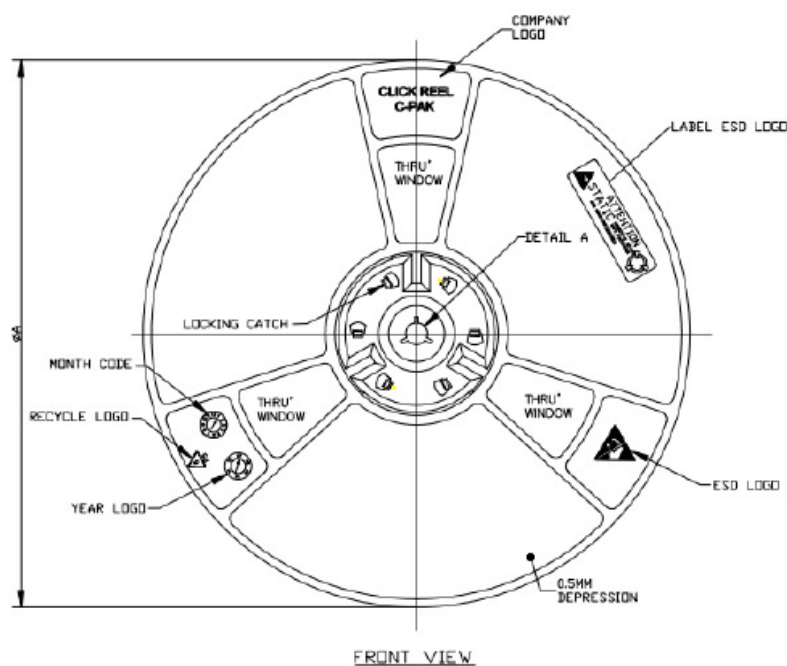
< Fig : Carrier Drawing >



< Fig : Pin1 Orientation >



Using 13" 4Hub Reel – [No 7" reel for such carrier width]
Reel Width – 12mm



7. Legal disclaimer

7.1. Warranty and Liability Disclaimer

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7.3. Disclaimer Regarding Changes

iSentek reserves the right to modify the contents of this datasheet, including specifications and descriptions, at any time and without prior notice. This document supersedes all previously issued information.

Revision History

Rev.	Date	Content of Changes
1.00	August 1, 2023	Initial release
1.02	Feb. 26, 2024	Remove quartz crystal from the application circuits
1.03	Nov. 7, 2024	<ol style="list-style-type: none">1. Modify Applications: Add EV cable application and modify green energy inverter systems2. Add standard compliance: IEC62955:2018 – Hardware delay is needed3. Correct grammar of contents and text format4. Add descriptions for properties that are dependent on the magnetic core