

IST8505

**Advanced Omnipolar TMR Switch
with Ultralow Power Management
& Anti-Magnetic Shielding**

Preliminary Datasheet

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1. General Description

The IST8505 is a magnetic sensor with powerful output driving capabilities and a digital output. This innovative device combines a TMR sensor with excellent analog signal processing and a low-power oscillator to operate at supply voltages ranging from 1 to 3.6V. The device also incorporates power gating, a power-saving feature that turns off the digital and analog circuits by triggering a high power-gating signal when the eFuse is completely loaded.

Features

- Omnipolar (operating with the magnetic field of either north or south pole)
- Nano power consumption ideal for battery-powered applications
- Input voltage range: VDD = 1 - 3.6 V
- High sensitivity of TMR sensor
- Power-gating for saving energy
- Latch Function (anti-interference)
- Under voltage lockout (UVLO)
- 1.45 x 1.45 x 0.44 mm³ LGA-4 package
- RoHS, HF and TSCA compliant

Applications

Medical Devices

IoT and smart home devices for door/window sensors, proximity sensors

Smartwatches, fitness trackers, and other wearables

Security systems

Robotics applications

Consumer Electronics: smartphones, tablets, laptops etc.

2. Block Diagram, Package Dimensions, Pin Configuration, and Application Circuit

2.1. Block Diagram

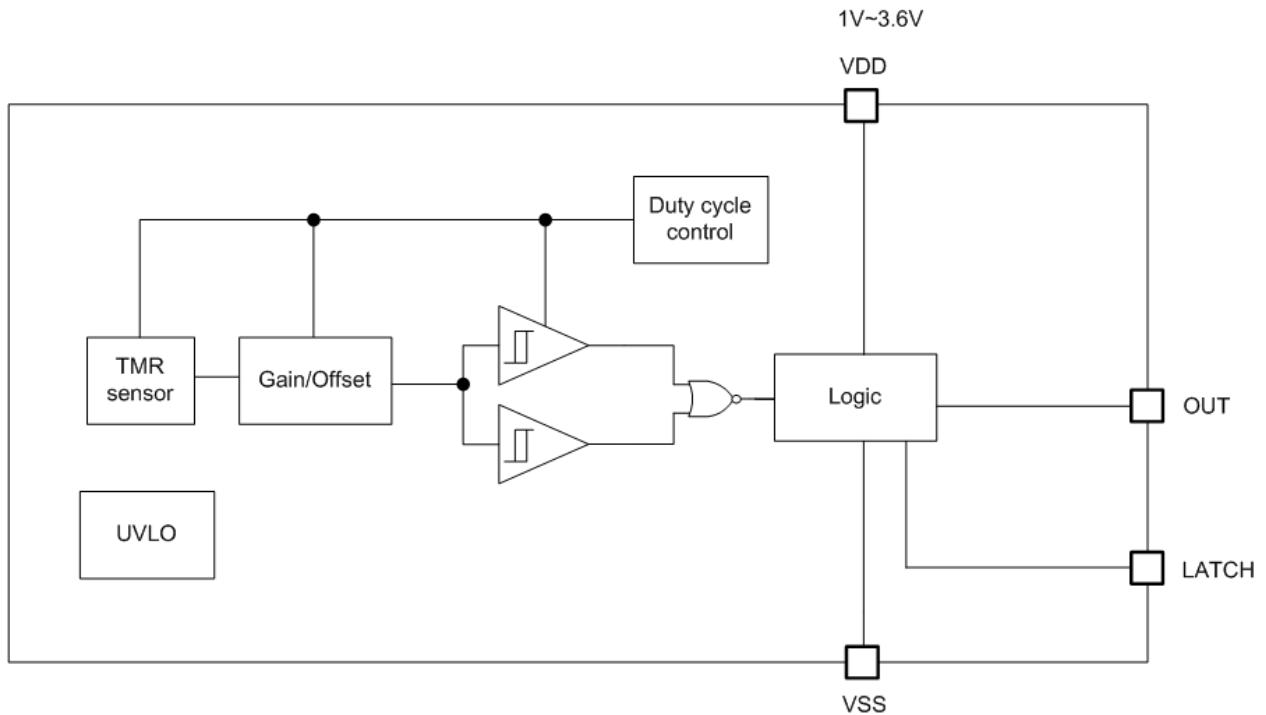


Figure 1. Block Diagram

2.2. Package Dimensions

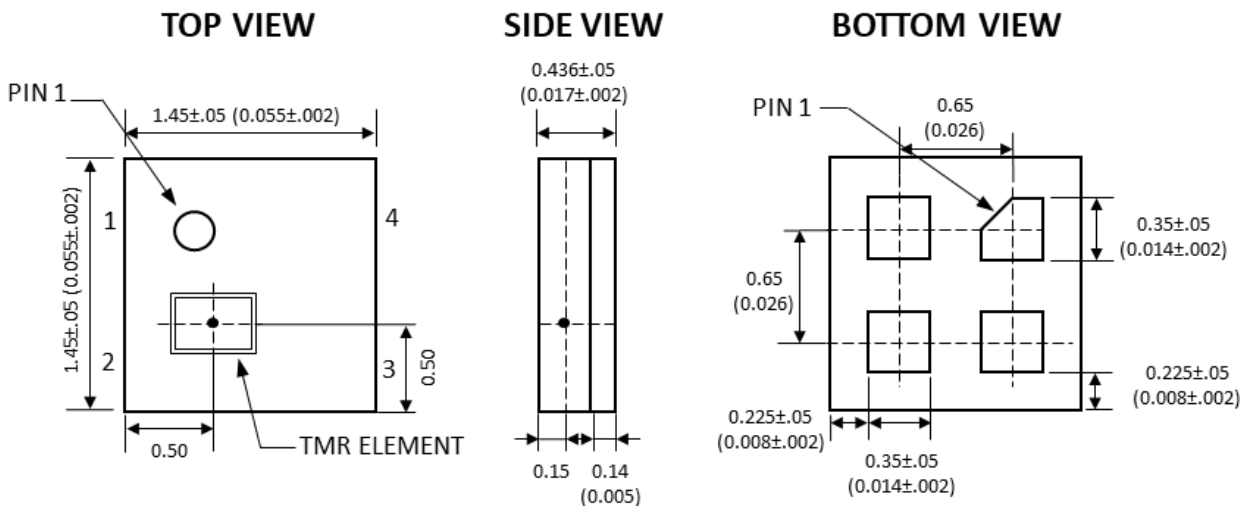


Figure 2. Package Dimension

2.3. Pin Configuration

Pin No.	Name	I/O Type	Description
1	LATCH	IO	Latch function
2	VDD	PWR	Power Supply Input
3	OUT	IO	Output
4	VSS	PWR	Ground

2.4. Axis of Sensitivity

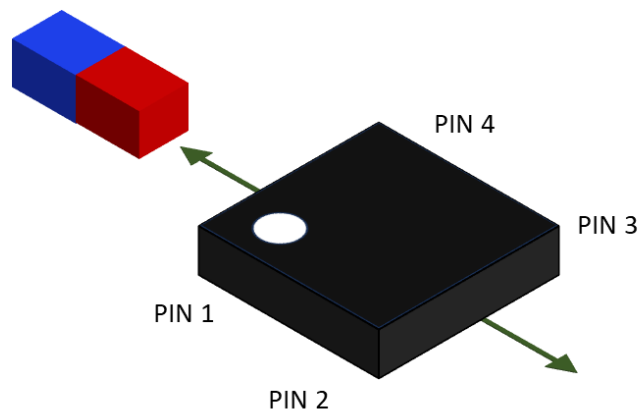


Figure 3. Axis of Sensitivity

2.5. Application Circuit

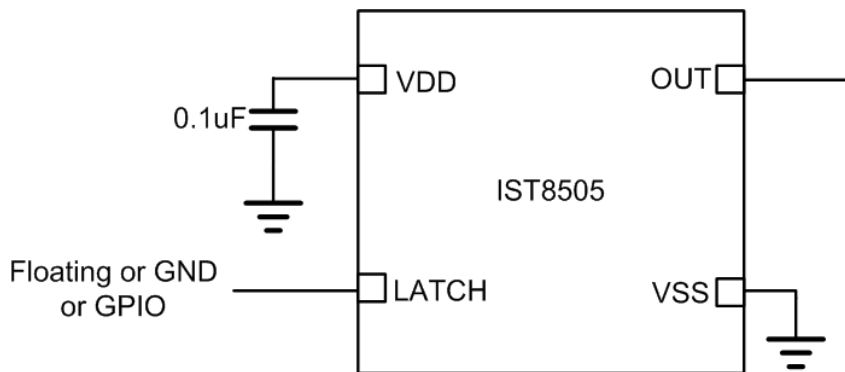


Figure 4. Application Circuit

Note on Output Latch Pin Behavior: When the Output Latch Pin (OLP) is not in use, it will remain in a floating state. This condition does not lead to an increase in current consumption, as the internal logic of the device defaults to a low state when the OLP is not engaged.

3. Electrical Specifications

3.1. Absolute Maximum Ratings

	MIN	MAX	UNIT
Power Supply Voltage	-0.3	3.6	V
Output Voltage	-0.3	$V_{DD} + 0.3$	V
Output Current		25	mA
Magnetic Flux Density		3000	G
Junction Temperature		125	°C
Storage Temperature	-65	150	°C

Note: Exceeding the absolute maximum ratings specified for this device can result in permanent damage. Furthermore, prolonged exposure to conditions at or near these absolute maximum ratings may adversely affect the device's reliability. Users are strongly advised to design their systems to avoid such extreme conditions to ensure long-term performance and reliability.

3.2. ESD Ratings

Symbol	Parameter	Description	Value	Unit
VESD	Electrostatic Discharge	Human Body Model (HBM), ANSI/ESDA/JEDEC JS-001	± 4000	V
		Charge-Device Model (CDM), JEDEC Specification & JEDEC JS-002	± 500	V

3.3. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	1	1.5	3.6	V
V_O	Output Voltage	0		V_{DD}	V
I_o	Output Current			25	mA
T_A	Operating Ambient Temperature	-40		85	°C

3.4. Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R _{ON}	PMOS Output Impedance			5	10	Ω
I _{DD(PK)}	Peak Current (active time)				200	μA
	Peak Current (output transition)	V _{DD} = 3.6V		7		mA
I _{DD(ST)}	Power up Current Consumption			60	100	μA
t _{ACTIVE}	Active Time Period			35		μs
f _s	Frequency of Magnetic Sampling		0.5	1	2	Hz
	Temperature Drift of Sampling	-40 - 85°C	-50		50	%
	Sensitivity of VDD	1 - 3.6 V	-20		20	%
T _s	Period of Magnetic Sampling			1000		ms
P _{GT}	Power Gating Time	Start from UVLO		1	3	ms
I _{DD(AVG)}	Average Current Consumption	V _{DD} = 1 V		10		nA
		V _{DD} = 1.5 V		11		
		V _{DD} = 3.6 V		20		
	UVLO, Rising V _{DD}		0.856	0.945	1.0	V
	UVLO, Falling V _{DD}		0.796	0.868	0.919	V
	UVLO, Hysteresis		60	77	92	mV
V _{OH}	High Level Output Voltage	I _{OUT} =15mA	0.91		3.55	V
V _{OL}	Low Level Output Voltage	I _{OUT} =50uA			0.2	V
V _{IL}	Latch Pin Input Low Voltage				VDD x 0.3	V
V _{IH}	Latch Pin Input High Voltage		VDD x 0.6		VDD	V

3.5. Magnetic Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
B _{OP}	Magnetic Threshold Operate Point	±5	±7	±10	Gauss
B _{RP}	Magnetic Threshold Release Point	±2	±3	±6	Gauss
B _{HYS}	Magnetic Hysteresis: B _{OP} -B _{RP}	3	4		Gauss

Note: This magnetic characteristic needs to be trimmed at the final test.

3.6. Magnetic Response Characteristics Under Different Temperatures

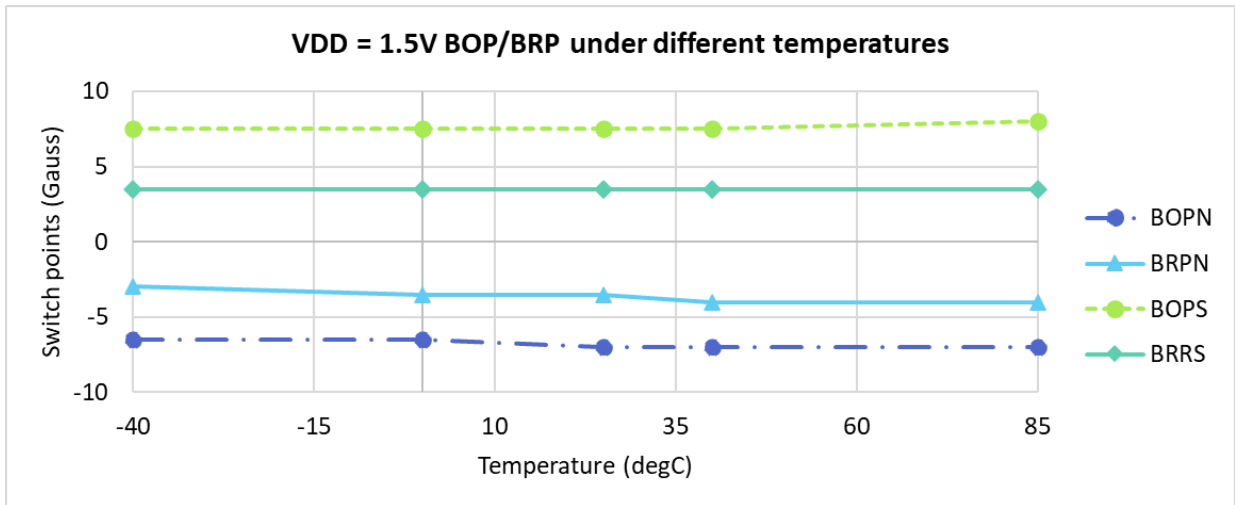


Figure 5. BOP/BRP at different temperatures, $V_{DD} = 1.5V$

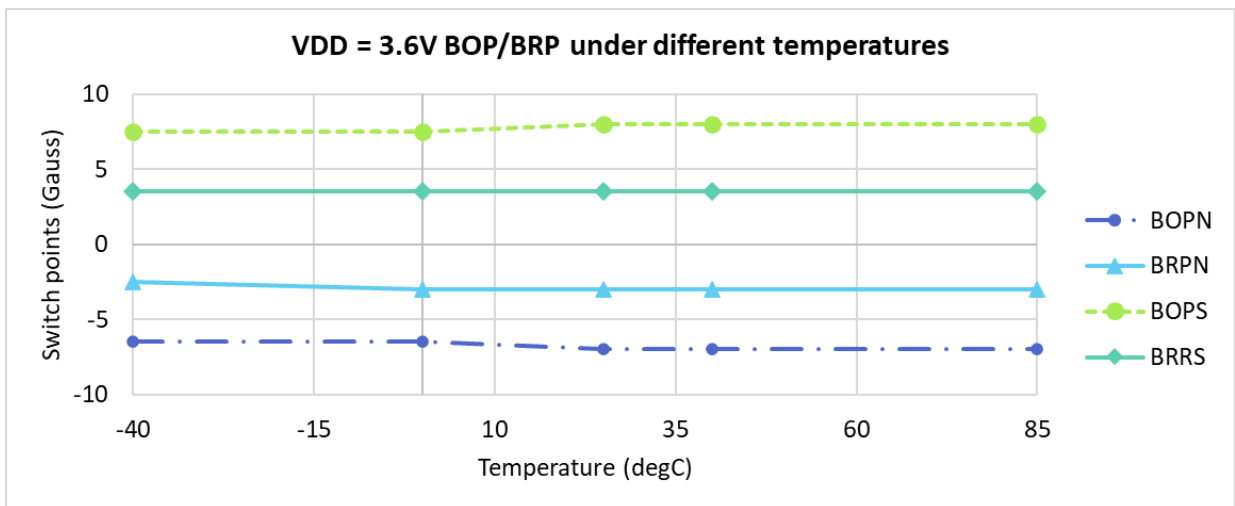


Figure 6. BOP/BRP at different temperatures, $V_{DD} = 3.6V$

3.7. Current Consumption Characteristics Under Different Temperatures

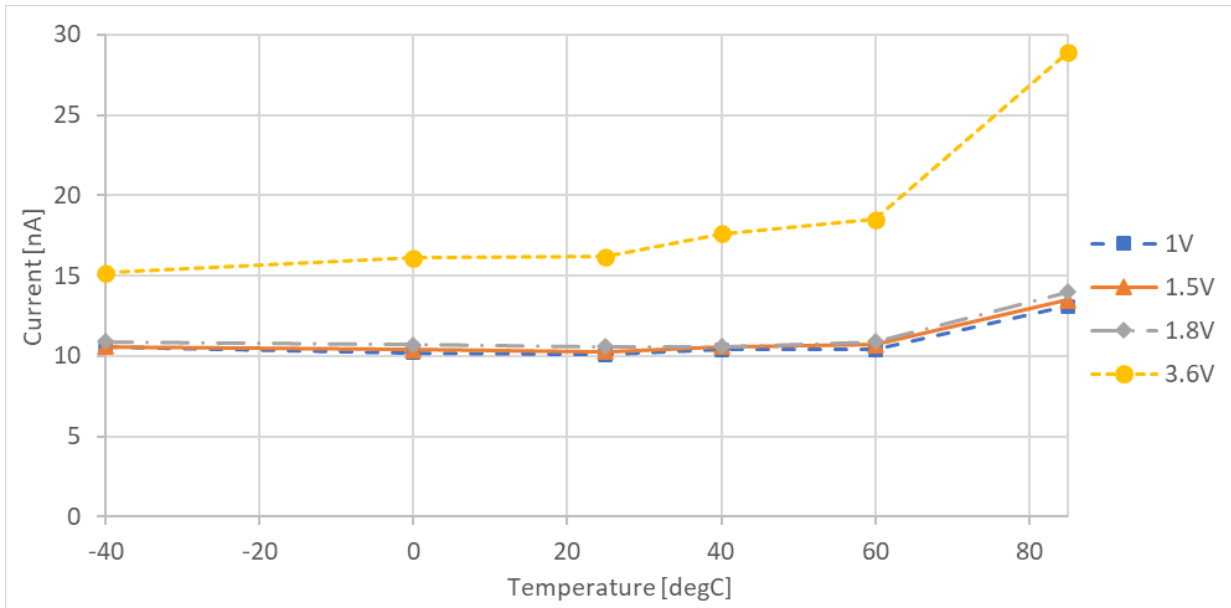


Figure 7. Current consumption at different temperatures, $V_{DD} = 1 - 3.6V$

3.8. Magnetic Response Characteristics at Different Supply Voltages

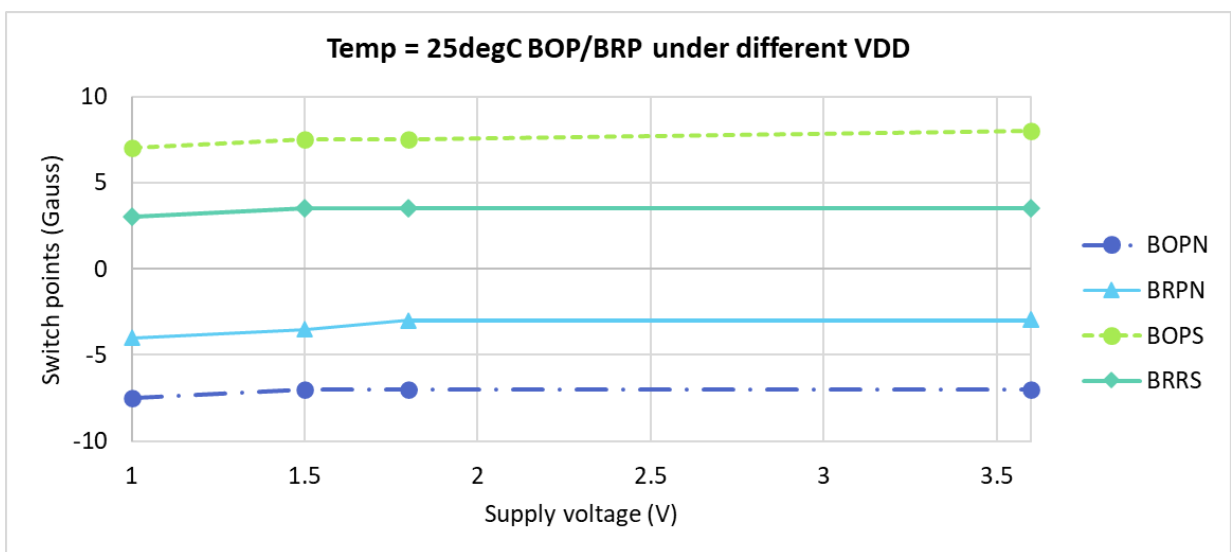


Figure 8. BOP/BRP at $V_{DD} = 1 - 3.6V$, $T = 25^{\circ}C$

3.9. Voltage and Current Output at Logic High Across Various Supply Voltages

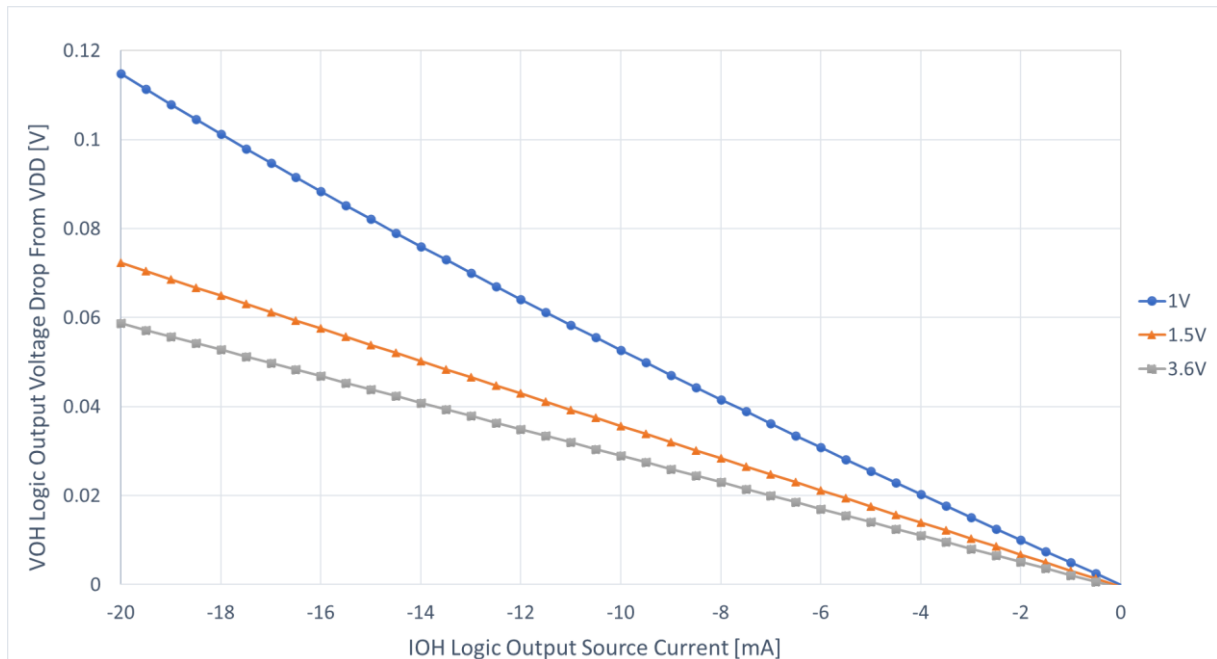


Figure 9. Voltage (VOH) and current (IOH) at logic high output for supply voltages ranging from 1V to 3.6V at 25°C ambient temperature

3.10. Voltage and Current Output at Logic Low Across Various Supply Voltages

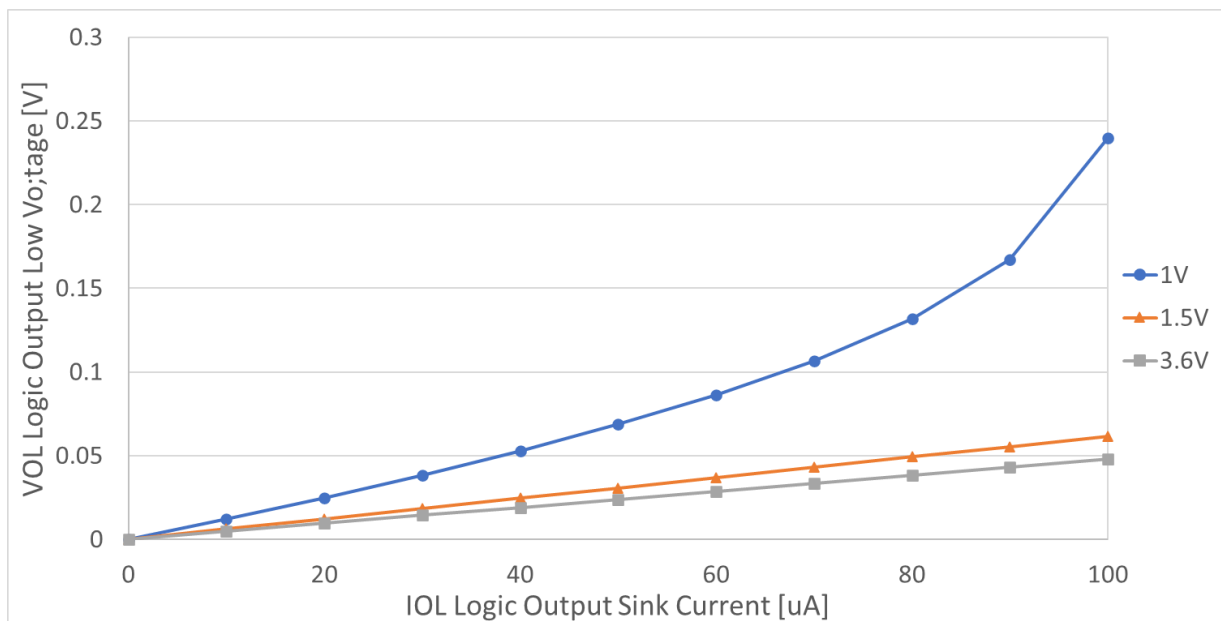


Figure 10. Voltage (VOL) and current (IOL) at logic low output for supply voltages ranging from 1V to 3.6V at 25°C ambient temperature

4. Recommended Reflow Profile

Based on the IPC/JEDEC joint industry standard, J-STD-020D-01, below is the temperature profile for moisture sensitivity characterization that is recommended.

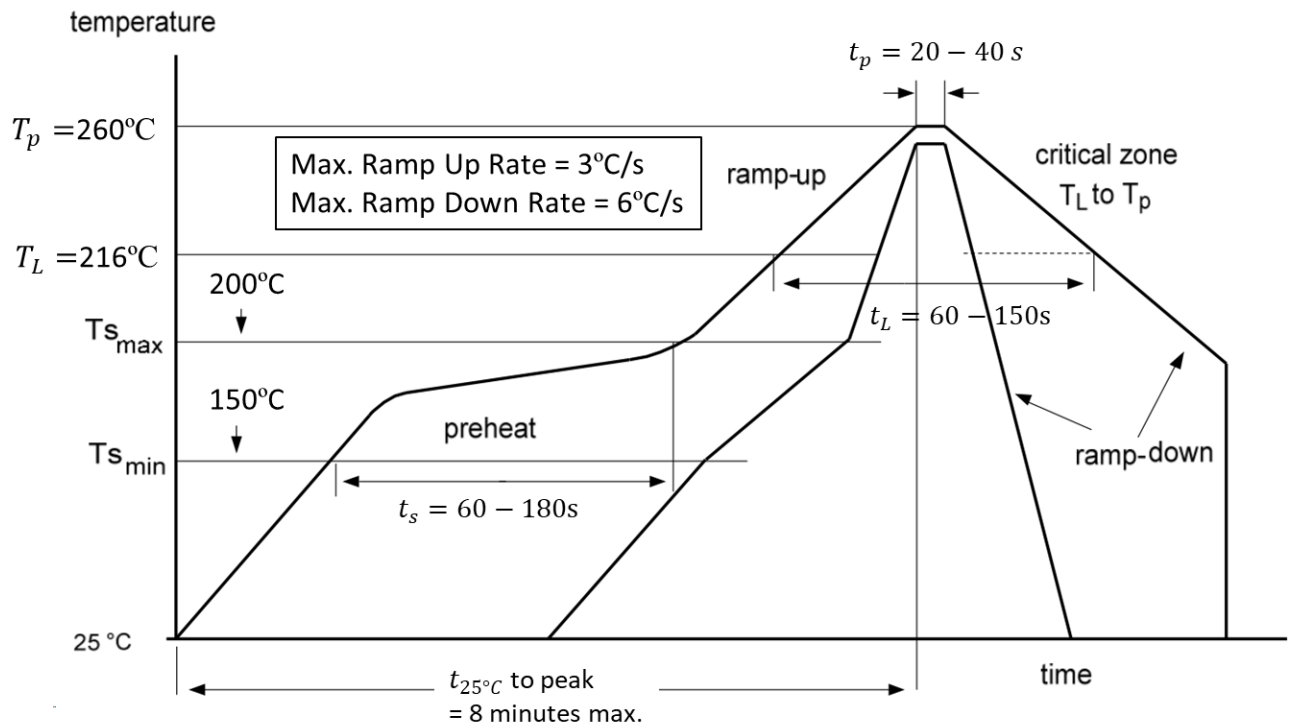


Figure 9. Suggested reflowing profile

Notes:

- Number of allowed reflow cycles: 3.
- Pb-free assembly data on base of SnAg3.8Cu0.7 (SAC)
- Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

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5. Protocol

5.1. Magnetic Response

When the magnetic field is present, the output will be low. Conversely, removing the magnetic field will result in a high output due to its high drive capacity.

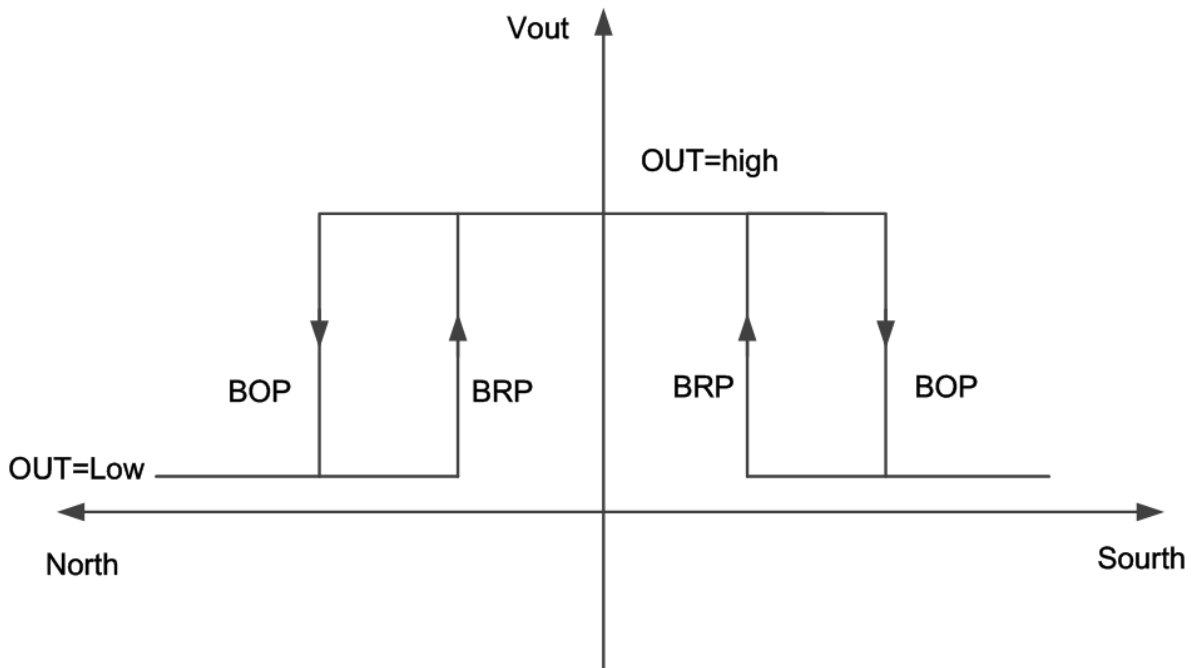


Figure 10. Magnetic Response

5.2. Output Type

The device has a push-pull CMOS output that can drive a high current output.

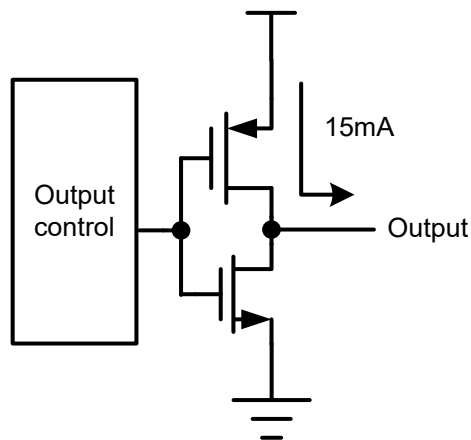


Figure 11. Output Type

5.3. Timing

Power Gating is a function for saving power consumption. It enables when UVLO ends, and the time interval is P_{GT} .

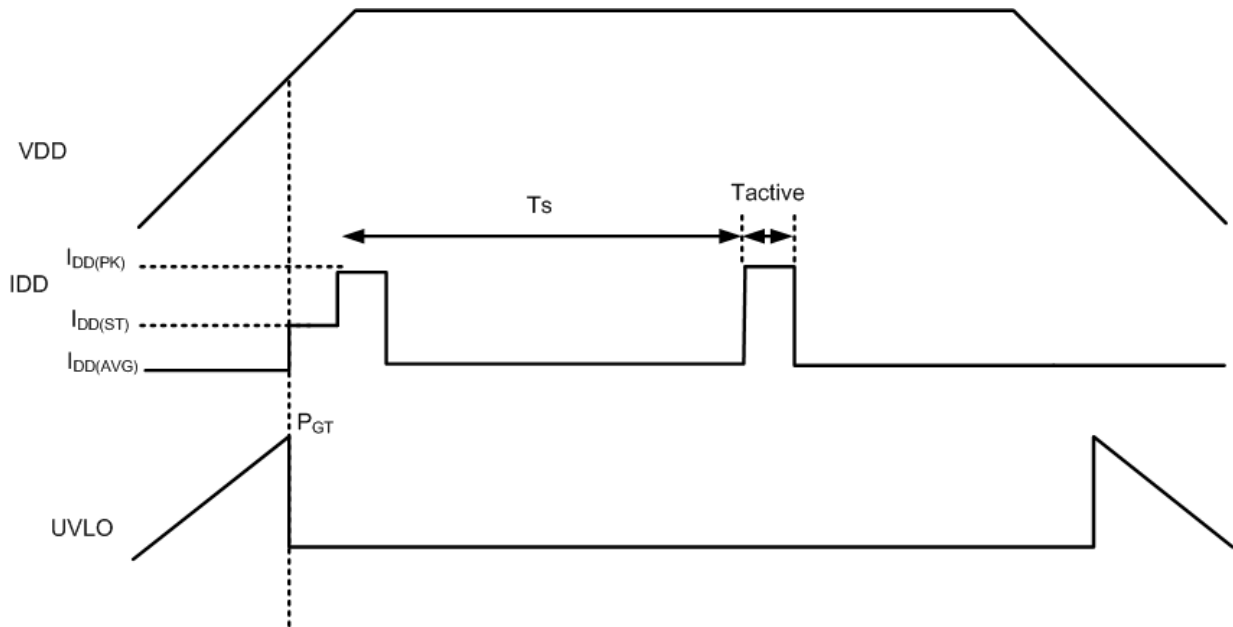


Figure 12. Normal Operation

5.4. Latch Function

IST8505 is a highly advanced and precision-engineered magnetic sensor designed to deliver accurate and dependable magnetic field detection across a wide range of applications. This datasheet section provides a comprehensive overview of the Latch Pin function, a critical feature of the TMR Magnetic Switch 8505, enabling users to exercise precise control over the sensor's output stability.

The IST8505 is equipped with a Latch Pin, a versatile feature that allows users to govern the output state of the sensor. When the Latch Pin is enabled (transitioning from Low to High), the sensor's output becomes fixed, ensuring it remains unaffected by any changes in the external magnetic field.

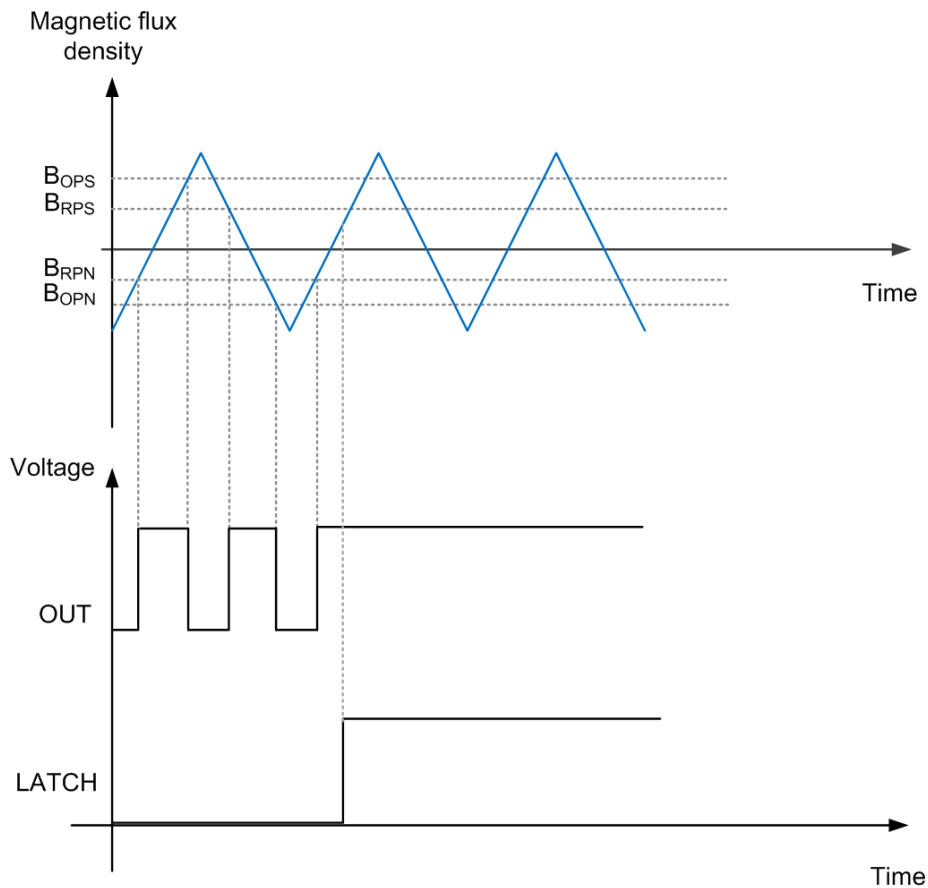


Figure 13. Latch Pin Operation

The Latch Pin function operates as follows:

- **Latch Pin Control:**

The Latch Pin can be manipulated through a General-Purpose Input/Output (GPIO) signal, giving users complete control over when to enable or disable output locking.

- **Output Locking:**

When the Latch Pin transitions from Low to High, the sensor locks its output state to its current value. The locked output remains unaffected by further changes in the magnetic field, providing a stable and reliable reading.

- **Output Reversion:**

To restore the sensor's output to its dynamic state, responsive to changes in the magnetic field, simply disable the Latch Pin by transitioning it from High to Low.

5.5. UVLO Operation

The UVLO function is a crucial feature of the IST8505, designed to ensure the reliable operation of the device even under challenging voltage conditions. UVLO is a power management feature that safeguards the device from erratic behavior and potential damage due to low supply voltage.

The UVLO function monitors the input voltage and prevents the device from operating

when the supply voltage falls below a predefined threshold (Rising V_{DD})

When the supply voltage (V_{DD}) falls below the UVLO threshold (Falling V_{DD}), the IST8505 goes into a low-power mode and ceases its normal operation. The UVLO function is enabled once the supply voltage is restored above the UVLO threshold, facilitating a controlled restart of the device.

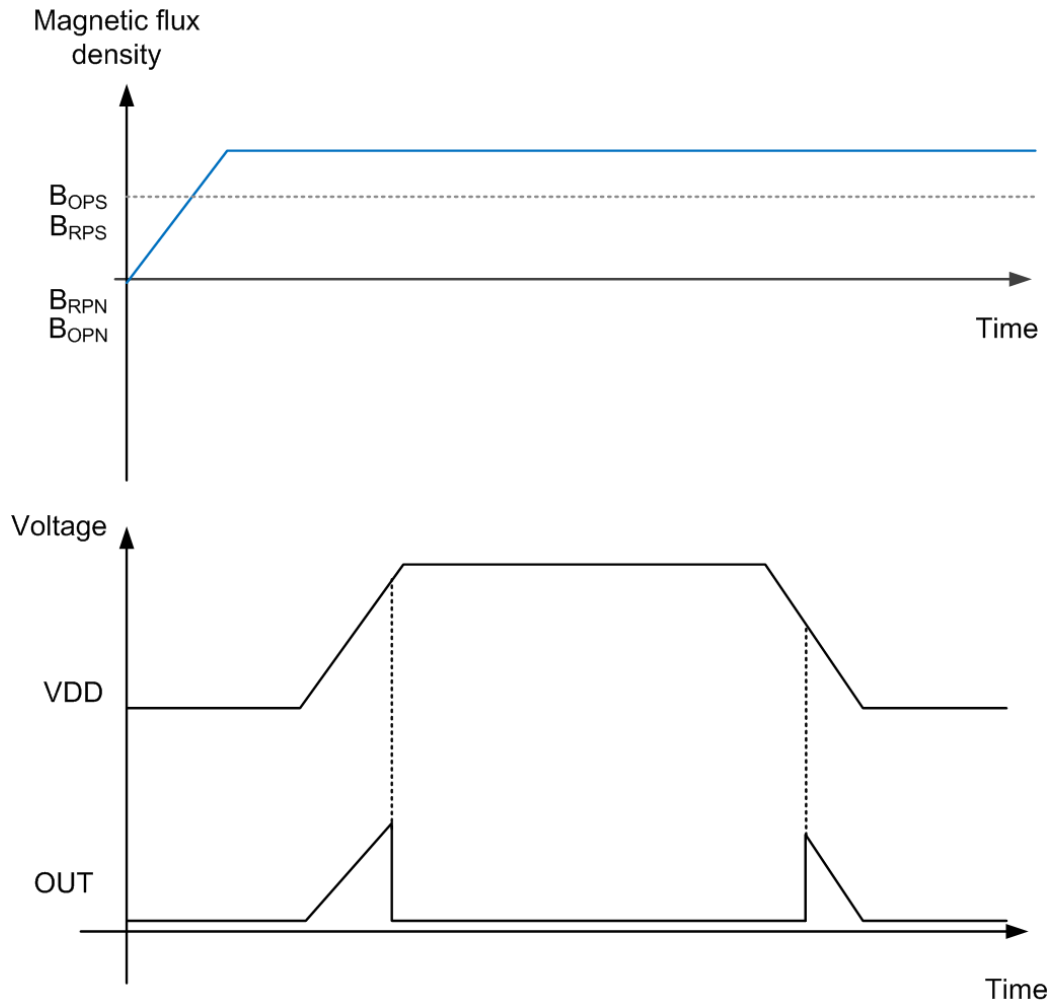
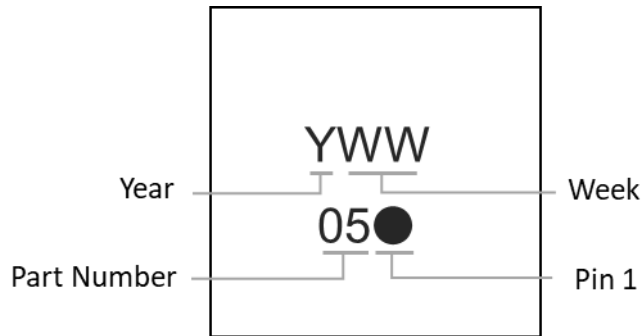


Figure 13. UVLO Operation

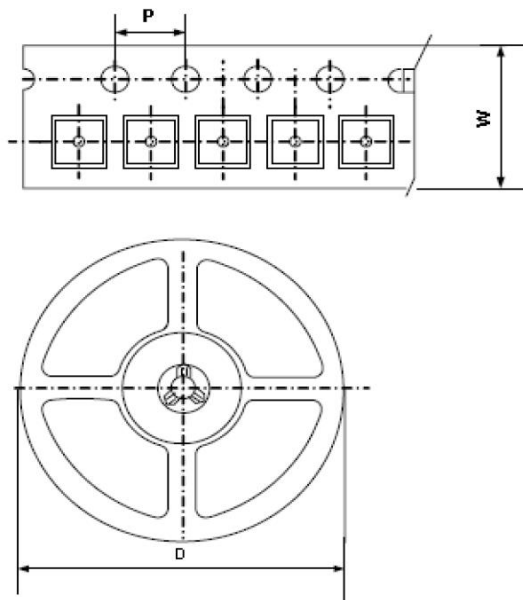
The UVLO function provides the following benefits:

- **Protection:** It prevents the IST8505 from operating when the supply voltage is insufficient to ensure reliable and accurate sensor functionality.
- **Low-Power Mode:** During UVLO, the device enters a low-power mode to minimize power consumption, ensuring efficient use of power resources.
- **Restoration:** The device will automatically resume normal operation when the supply voltage rises above the UVLO threshold, without the need for manual intervention.

6. Marking Information



7. Packing Information



Package Type	Carrier Width (W)	Pitch (P)	Reel Size (D)	Packaging Minimum
LGA-4	8.0 ± 0.3 mm	4.0 ± 0.1 mm	178 ± 1 mm	Tape and Reel: 3k pcs per reel

For more information on iSentek’s magnetic sensors, please send an email to sales@isentek.com or visit our website at www.isentek.com.

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